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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,706	07/31/2003	Yoshiro Mikami	500.41297CX1	1602

20457 7590 09/20/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,706	MIKAMI ET AL.	
	Examiner	Art Unit	
	Regina Liang	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/083,548.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9-7-05, 11-8-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 recites the limitation "said power supply control element" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,611,107. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims 1-14 of this application and claims 1-15 of U.S. Patent No. 6,611,107 are claiming an image display apparatus having plurality of memory

control circuits for controlling and driving the plurality of current driven display elements.

The following is an example for comparing claim 1 of this application and claim 1 of US. PAT. NO. 6,611,107.

claim 1 of this application	claim 1 of US. PAT. NO. 6,611,107
an image display apparatus comprising: a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;	an image display apparatus comprising: a plurality of scanning wires distributively arranged in an image display region for transmitting a scanning signal;
a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;	a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;
a plurality of current driven electro-optical display elements each arranged in a pixel region surrounded by said scanning wires and said signal wires connected to a common power supply;	a plurality of current driven electro-optical display elements each arranged in a pixel region surrounded by each said scanning wire and each said signal wire and connected to a common power supply;
a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements;	a plurality of driving elements each connected in series with each said electro-optical display element, connected to said common power

	supply, and applied with a bias voltage to drive each said electro-optical display element for display;
a plurality of memory control circuits for holding said signal voltage in response to said scanning signal to control driving of said driving elements based on said held signal voltage, wherein said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each of said driving elements, and subsequently applies said driving elements with the held signal voltage as said bias voltage.	a plurality of memory control circuits each for holding said signal voltage in response to said scanning signal to control driving of each said driving element based on said held signal voltage, wherein each said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each said driving element, and subsequently applies each said driving element with said held signal voltage as said bias voltage.

As can be seen above, claim 1 is this application is similar to claim 1 of US. PAT. NO. 6,611,107, and claim 1 of this application is broader version of claim 1 of US. PAT. NO. 6,611,107.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Komiya (US. PAT. NO. 6,509,692).

As to claim 1, Figs. 1 and 7 of Komiya discloses an image display apparatus comprising: a plurality of scanning wires (gate lines 1); a plurality of signal wires (data line 2); a plurality of current driven electro-optical display elements (organic EL 7) each arranged in a pixel region surrounded by the scanning wires and the signal wires connected to a common power supply (driving lines 3 is connected to a power source PV); a plurality of driving elements (driving TFT 6) arranged in the pixel region connected with the display elements (organic EL 7). Komiya also discloses the apparatus having a plurality of memory control circuits (selection transistors 4 and storage capacitor 5 corresponding memory control circuits) for holding the signal voltage in response to the scanning signal to control driving of the driving elements based on the held signal voltage, and the memory control circuit samples and holds the signal voltage while blocking a bias voltage from being applied to each of the driving elements, and subsequently applies the driving elements with the held signal voltage as the bias voltage (referring to Fig. 1 for example, in response to the scanning signal on gate line 1, selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection

transistors 4, and charged and held on the storage capacitor 5, see col. 1, line 47 to col. 2, lines 12 for example).

As to claim 2, Komiya teaches the driving lines 3 is connected to a power source PV for supplying or stop supplying the power to the driving elements.

As to claim 3, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal for scanning line (1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 4, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode).

As to claim 5, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

As to claim 6, note the discussion of claim 1 above. In addition, Komiya (Fig. 1 for example) teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to a voltage applied to the driving elements in a sampling period, in this

period, no voltage is applied to the driving element. Komiya also teaches when the driving transistor 6 is closed, the signal voltage held on the capacitor is applied to the driving transistor 6, this corresponds to the voltage applied to the driving elements in a write period. Thus, Komiya teaches the voltage applied to the driving elements in a sampling period is lower than a voltage in a write period.

As to claim 7, Komiya teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to the driving elements (driving transistor 6) are non-conductive in a sampling period.

As to claim 8, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 9, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode.

As to claim 10, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

As to claim11, note the discussion of claim 1 above. In addition, Komiya (Fig. 1 for example) teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to a voltage applied to the driving elements in a sampling period, in this period, no electric power is applied to the driving element since the driving transistors 6 are opened. Komiya also teaches when the driving transistor 6 is closed, the signal voltage held on the capacitor is applied to the driving transistor, this corresponds to the voltage applied to the driving elements in a write period, in this period, the electric power are supplied to the driving elements since the driving transistors 6 are closed. Thus, Komiya teaches the electric power supplied to the driving elements (transistor 6) in a sampling period is lower than the electric power in a write period.

As to claim 12, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 13, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the

main sampling switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode.

As to claim 14, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sekiya et al (US. PAT. NO. 6,583,775), Sanford et al (US. PAT. NO. 6,734,636), Bae (US. PAT. NO. 6,570,338).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

9/16/05